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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,562	11/21/2003	Akira Ishikawa	740756-2669	8458

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EXAMINER	
NGUYEN, JOSEPH H	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,562	ISHIKAWA ET AL.	
	Examiner	Art Unit	
	Joseph Nguyen	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-26* is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/21/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: numerals 1, 2a, 2b, 2c are not shown in figure 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 6, 8, 11-14, 18-20 are rejected under 35 U.S.C. 102(a) as being anticipated by the acknowledged prior art (APA) as shown in figure 6 of the present application.

Regarding claim 1, applicant disclosed on figure 6 a semiconductor device comprising a pixel region 101; a peripheral circuit region 102 placed in at least a part of an area surrounding the pixel region; gate electrodes of TFT's formed in the peripheral circuit region (pages 1-2 of the present application); and a wiring connected to the gate electrodes and formed in a layer over the gate electrodes (page 2 of the present application); wherein the gate electrodes in different TFT's are isolated from one another. Note that the term "isolated" is hereby interpreted as "physically isolated".

Regarding claim 2, applicant disclosed on figure 6 the wiring is a multilayer wiring having two or more layers (lines 7-10 of page 2 of the present application).

Regarding claim 3, applicant disclosed on figure 6 applicant disclosed on figure 6 a semiconductor device comprising a pixel region 101; a peripheral circuit region 102

placed in at least a part of an area surrounding the pixel region; gate electrodes of TFT's formed in the peripheral circuit region (pages 1-2 of the present application); and a short distance wiring connected to the gate electrodes and formed in a layer over the gate electrodes (page 2 of the present application); wherein the gate electrodes in different TFT's are isolated from one another.

Note that the term "short distance" is merely a label. Since this so-called short distance wiring is not defined in a specific dimension, any wiring can be interpreted as a short distance wiring herein.

Regarding claim 4, applicant disclosed on figure 6 the short distance wiring is a wiring for leading one functional block.

Regarding claim 6, applicant disclosed on figure 6 the short distance wiring is a multilayer wiring having two or more layers (lines 7-10 of page 2 of the present application).

Regarding claim 8, applicant disclosed on figure 6 applicant disclosed on figure 6 a semiconductor device comprising a pixel region 101; a peripheral circuit region 102 placed in at least a part of an area surrounding the pixel region; gate electrodes of TFT's formed in the peripheral circuit region (pages 1-2 of the present application); and a long distance wiring connected to the gate electrodes and formed in a layer over the gate electrodes (page 2 of the present application); wherein the gate electrodes in different TFT's are isolated from one another.

Note that the term "long distance" is merely a label. Since this so-called long distance wiring is not defined in a specific dimension, any wiring can be interpreted as a long distance wiring herein.

Regarding claim 11, applicant disclosed on figure 6 the long distance wiring is a multilayer wiring having two or more layers (lines 7-10 of page 2 of the present application).

Regarding claims 12-14, applicant disclosed that at least one of the layers of the multilayer wiring is formed from a low resistance material (lines 7-10 of page 2 of the present application).

Regarding claims 18-20, applicant disclosed on figure 6 a transistor is formed in the peripheral circuit region, and wherein a multilayer wiring having two or more layers is formed over the transistor (lines 7-10 of page 2 of the present application).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 9 and 10 rejected under 35 U.S.C. 103(a) as being unpatentable over (APA) as applied to claims 3 and 8 above.

Regarding claim 5, applicant disclosed on figure 6 substantially all the structure set forth in the claimed invention except the short distance wiring being 2 μm or longer

and short than 2 cm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having the short distance wiring being 2 μm or longer and short than 2 cm for the purpose of improving the performance of a semiconductor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 9, applicant disclosed on figure 6 substantially all the structure set forth in the claimed invention except the long distance wiring being hundred times longer than the pixel pitch. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having the long distance wiring being hundred times longer than the pixel pitch for the purpose of improving the performance of a semiconductor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 10, applicant disclosed on figure 6 substantially all the structure set forth in the claimed invention except the long distance wiring being 2 cm or longer and short than 10 cm. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having the long distance wiring being 2 cm or longer and short than 10 cm for the purpose of improving the performance of a semiconductor device, since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over (APA) as applied to claim 3 above, and further in view of Yamazaki et al.

Regarding claim 7, applicant disclosed on figure 6 substantially all the structure set forth in the claimed invention except a long distance wiring formed in a layer over the short distance wiring. However, Yamazaki et al. discloses on figure 8C a long distance wiring formed in a layer over the short distance wiring (elements above the gate on the left side of figure 8C). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having a long distance wiring formed in a layer over the short distance wiring for the purpose of improving the electrical connection within a semiconductor device.

Claims 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over (APA) as applied to claims 12-14 above, and further in view of Hamada et al..

Regarding claim 15-18, applicant disclosed on figure 6 substantially all the structure set forth in the claimed invention except the low resistance material being one material from the group consisting of copper. However, Hamada et al. teaches that the low resistance material from the group consisting of copper ([Para. 0195]). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify (APA) by having the low resistance material being one material from the group consisting of copper for the purpose of raising the current density of a wiring line as taught by Hamada et al. ([Para. 0195]).

Allowable Subject Matter

Claims 21-26 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
January 16, 2005

ALLAN R. WILSON
PRIMARY EXAMINER